Abstracts

A 5.8-GHz two-stage high-linearity low-voltage low noise amplifier in a 0.35-/spl mu/m CMOS technology [WLANs]

Ren-Chieh Liu, Chung-Rung Lee, Huei Wang and Chorng-Kuang Wang. "A 5.8-GHz two-stage high-linearity low-voltage low noise amplifier in a 0.35-/spl mu/m CMOS technology [WLANs]." 2002 Radio Frequency Integrated Circuits (RFIC) Symposium 02. (2002 [RFIC]): 221-224.

A 5.8-GHz two-stage high-linearity low-voltage CMOS low-nose amplifier (LNA) has been developed in a 0.35-/spl mu/m pure digital CMOS technology without any additional mask or post-processing steps. A two-stage architecture is used to simultaneously optimize the gain and noise performance. Based on the modified CMOS model valid for RF range, the LNA with fully on-chip input, output and inter-stage matching was designed to verify the two-stage LNA architecture. This LNA chip achieves measured results of 3.2-dB NF, +6.7-dBm IIP3 and -3.7-dBm output P/sub 1dB/ at 5.8 GHz. A figure-of-merit for linearity (output IP3/P/sub DC/) of 1.2 is achieved, which is believed to be among the best reported for a CMOS low-noise amplifier operating at 5-6 GHz ISM band. The effective circuit area is only 0.63 /spl times/ 0.46 mm/sup 2/.

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